What is claimed is:

1. A package substrate for improving electrical performance comprising:

a first insulating layer having a top surface and a bottom surface;

a plurality of groups of inner fingers formed on the top surface of the first insulating layer for electrically connecting to a chip;

a plurality of outer fingers formed on the top surface of the first insulating layer for electrically connecting to the chip;

a plurality of outer through holes formed through the first insulating layer and electrically connected to the corresponding outer fingers;

a plurality of inner through holes formed through the first insulating layer and electrically connected to the corresponding inner fingers; and

a ground/power layer disposed on the bottom surface of the first insulating layer, wherein the ground/power layer has a plurality of openings, and the inner through holes are crowded in groups to pass through the openings which are electrically isolated from the ground/power layer.

2. The substrate in accordance with claim 1, wherein a distance between the two adjacent openings is not less than 0.2mm.

3. The substrate in accordance with claim 1, wherein the ground/power layer between two adjacent openings is in strip shape.

4. The substrate in accordance with claim 1, wherein each group of inner through holes pass through the corresponding openings and arranged in grid array.

5. The substrate in accordance with claim 1, wherein the top surface of the first insulating layer includes a chip-attaching region.

6. The substrate in accordance with claim 5, wherein the openings are radially oriented to the chip-attaching region.

7. The substrate in accordance with claim 5, further comprising a metal ring formed on the top surface of the first insulating layer between the chip-attaching region and the

inner fingers.

8. The substrate in accordance with claim 1, further comprising a second insulating layer formed on the bottom surface of the first insulating layer to sandwich the ground/power layer.

9. The substrate in accordance with claim 8, further comprising another ground/power layer on the bottom surface of the second insulating layer.

10. A package substrate for improving electrical performance comprising:

a first insulating layer having a top surface and a bottom surface;

a plurality of inner fingers formed on the top surface of the first insulating layer for electrically connecting a chip;

a plurality of outer fingers formed on the top surface of the first insulating layer for electrically connecting the chip;

a plurality of outer through holes formed through the first insulating layer and electrically connected with corresponding outer fingers;

a plurality of inner through holes formed through the first insulating layer and electrically connected with corresponding inner fingers; and

a first ground/power layer disposed on the bottom surface of the first insulating layer, wherein the first ground /power layer has a plurality of openings, at least one of the inner through holes passes through each opening with electrical isolation from the first ground/power layer in a manner that the openings are crowded in groups for improving electrical performance.

11. The substrate in accordance with claim 10, wherein the first ground/power layer between two adjacent groups of the openings is in strip shape.

12. The substrate in accordance with claim 11, wherein the strip-shaped first ground/power layer is not less than 0.2mm in width.

13. The substrate in accordance with claim 10, wherein the plurality of openings are formed on the first ground/power layer in radial arrangement.

14. The substrate in accordance with claim 10, wherein the top surface of the first insulating layer includes a chip-attaching region.

15. The substrate in accordance with claim 14, further comprising a metal ring formed on the top surface of the first insulating layer between the inner fingers and the chip-attaching region.

16. The substrate in accordance with claim 15, wherein the metal ring is electrically connected with the first ground /power layer.

17. The substrate in accordance with claim 10, further comprising a second insulating layer formed on the bottom surface of the first insulating layer to sandwich the first ground/power layer.

18. The substrate in accordance with claim 17, further comprising a second ground/power layer on the bottom surface of the second insulating layer.